State of the Art VME Digitizers: ADC, QDC, TDC

Common Features:

- Zero suppression with individual thresholds
- Multicast for event reset and timestamping start
- Supports different types of time stamping
- Independent bank operation
- Address modes: A24 / A32
- Data transfer modes: D16 (registers), D32, BLT32, MBLT64, CBLT, CMBLT64
- mesytec control bus for remote control of external mesytec modules
- Live insertion (can be inserted in a running crate)
- +5V, +/- 12 V needed

MADC-32:
High precision peak sensing ADC:

- High quality 11 to 13 bit (2, 4, 8 k) conversion with sliding scale ADC
- 800 ns, 1.6 us, 6.4 us conversion time for 32 channels with 2 k, 4 k, 8 k resolution.
- 8 k (32 bit-) words multi event buffer (1 word = 1 converted channel => 240 ... 2730 events total)
- Two builtin register adjustable gate generators
- Input range, register selectable 4 V, 8 V, 10 V

MTDC-32:
High resolution 10 ps time digitizer:

- 32 + 2 channel time stamping TDC
- Start-stop mode with configurable window of interest, 16 bit conversion time stamper mode with 46 bit time stamp.
- Channel to channel or gate to channel TOF resolution better than 10 ps rms
- Conversion time 160 ns.
- 48 k (32 bit-) words multi event buffer
- Channel inputs and differential control inputs ECL, LVDS and PECL.
- Channel inputs can be jumpered to accept NIM, TTL or analog signals

MQDC-32:
Charge integrating ADC:

- High quality 12 bit (4 k) sliding scale ADC
- 250 ns conversion and clear time for 32 channels
- 64 k (32 bit-) words multi event buffer
- Analog Inputs AC coupled and baseline restored. (Optional DC coupled via register setting)
- Input configuration jumper selectable
- Individual Gate inputs: differential ECL, LVDS and PECL.
- Easy to use pulse shape analysis capability by 32 individual gate limiters (4 ns to 300 ns)
- Multiplicity filter
- Configurable: individual gates or common gate